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Terms	Documents
L26 and L12 and L13	0

Database: US Pre-Grant Publication Full-Text Database; **US Patents Full-Text Database**; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L28

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Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L28	L26 and l12 and l13	0	L28
L27	L26	98	L27
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L26	l25 and l23	123	L26
L25	address adj tag	3873	L25
DB=USPT; PLUR=YES; OP=OR			
L24	L23	344	L24
DB=PGPB,USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L23	l17 and L22	422	L23
L22	711/$.ccls.	23552	L22
L21	(6629205 or 6289420).pn.	3	L21
L20	l19 and l18	2	L20
L19	('6049856' |'6522565')!.ABPN1,NRPN,PN,TBAN,WKU.	4	L19
L18	l9 and l10 and l17	37	L18
L17	(reads or read or reading) with writ$ with l11 with l14	800	L17
L16	l12 same l13 same l14	0	L16
L15	l12 with l13 with L14	0	L15
L14	concurrent$ or parallel or simultaneous$ or ("same" adj time)	4217113	L14

L13	l11 near2 L10	162	L13
L12	l9 near2 L11	116	L12
L11	cache	80408	L11
L10	write near2 (portion or partial)	8145	L10
L9	read$ near2 (portion or partial)	39945	L9
L8	l7 and l6	3	L8
L7	unaligned	3168	L7
L6	horst-$.in.	3112	L6
L5	0365281.pn.	1	L5
L4	ep 0 365 281	17475744	L4
L3	('ep365281')!.ABPN1,NRPN,PN,TBAN,WKU.	0	L3
L2	('ep0365281')!.ABPN1,NRPN,PN,TBAN,WKU.	0	L2
L1	6289420.pn.	2	L1

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(concurrent <or> simultaneous <or> parallel) <and> rea Search

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Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **RAPID-Cache-A reliable and inexpensive write cache for high performance storage systems**
Yiming Hu; Nightingale, T.; Qing Yang;
Parallel and Distributed Systems, IEEE Transactions on , Volume: 13 , Issue: 3 , March 2002
Pages:290 - 307

[Abstract] [PDF Full-Text (1188 KB)] IEEE JNL

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2 **A cache coherence scheme suitable for massively parallel processors**
Baldwin, R.;
Supercomputing '93. Proceedings , 15-19 Nov. 1993
Pages:730 - 739

[Abstract] [PDF Full-Text (648 KB)] IEEE CNF

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3 **Dynamic SMP Clusters with Communication on the Fly in NoC Technology for Very Fine Grain Computations**
Tudruj, M.; Masko, L.;
Parallel and Distributed Computing, 2004. Third International Symposium on/Algorithms, Models and Tools for Parallel Computing on Heterogeneous Networks, 2004. Third International Workshop on , 05-07 July 2004
Pages:97 - 104

[Abstract] [PDF Full-Text (224 KB)] IEEE CNF

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4 **Communication on the fly and program execution control in a system of dynamically configurable SMP clusters**
Tudruj, M.; Masko, L.;
Parallel, Distributed and Network-Based Processing, 2003. Proceedings. Eleventh Euromicro Conference on , 5-7 Feb. 2003
Pages:67 - 74

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5 **Cache coherence in a multiport memory environment**

Crawford, S.E.; DeMara, R.F.;
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Pages:632 - 642

[Abstract] [PDF Full-Text (800 KB)] **IEEE CNF**

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6 **Global address space, non-uniform bandwidth: a memory system performance characterization of parallel systems**
Stricker, T.; Cross, T.;
High-Performance Computer Architecture, 1997., Third International Symposium on , 1-5 Feb. 1997
Pages:168 - 179

[Abstract] [PDF Full-Text (1292 KB)] **IEEE CNF**

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7 **Massively parallel algorithms for trace-driven cache simulations**
Nicol, D.M.; Greenberg, A.G.; Lubachevsky, B.D.;
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Pages:849 - 859

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Pages:66 - 70 vol.1

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9 **On some implementation issues for value prediction on wide-issue ILP processors**
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Pages:145 - 156

[Abstract] [PDF Full-Text (1048 KB)] **IEEE CNF**

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Nilsson, J.; Dahlgren, F.;
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Pages:684 - 692

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11 **The SPEED cache c herence protoc l f r an optical multi-access interconnect architecture**
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Massively Parallel Processing Using Optical Interconnections, 1995., Proceedings of the Second International Conference on , 23-24 Oct. 1995
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12 **Cache memory design f r the data transport to array processors**
Volkers, H.; Jeschke, H.; Wehberg, T.;
Circuits and Systems, 1990., IEEE International Symposium on , 1-3 May 1990
Pages:49 - 52 vol.1

[Abstract] [PDF Full-Text (376 KB)] **IEEE CNF**

13 **The impact of negative acknowledgments in shared memory scientific applications**
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[Abstract] [PDF Full-Text (1831 KB)] **IEEE JNL**

14 **A 32Kb SRAM cache using current mode operation and asynchronous wave-pipelined decoders**
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SOC Conference, 2004. Proceedings. IEEE International , 12-15 Sept. 2004
Pages:251 - 254

[Abstract] [PDF Full-Text (328 KB)] **IEEE CNF**

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Nakayama, M.; Sakakibara, H.; Kusunoki, M.; Kurita, K.; Yokoyama, Y.; Miyaoka, S.; Koike, J.; Tamba, N.; Kobayashi, T.; Kume, M.; Sawamoto, H.; Kawata, A.; Tanaka, H.; Takada, Y.; Yamamoto, M.; Yagyu, M.; Tsuchiya, Y.; Yoshida, H.; Kitamura, N.; Yamaguchi, K.;
Solid-State Circuits Conference, 2000. Digest of Technical Papers. ISSCC. 2000 IEEE International , 7-9 Feb. 2000
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[Abstract] [PDF Full-Text (363 KB)] **IEEE CNF**

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